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# NNJ-TPLLV1/A

Technical Notes

REV. H

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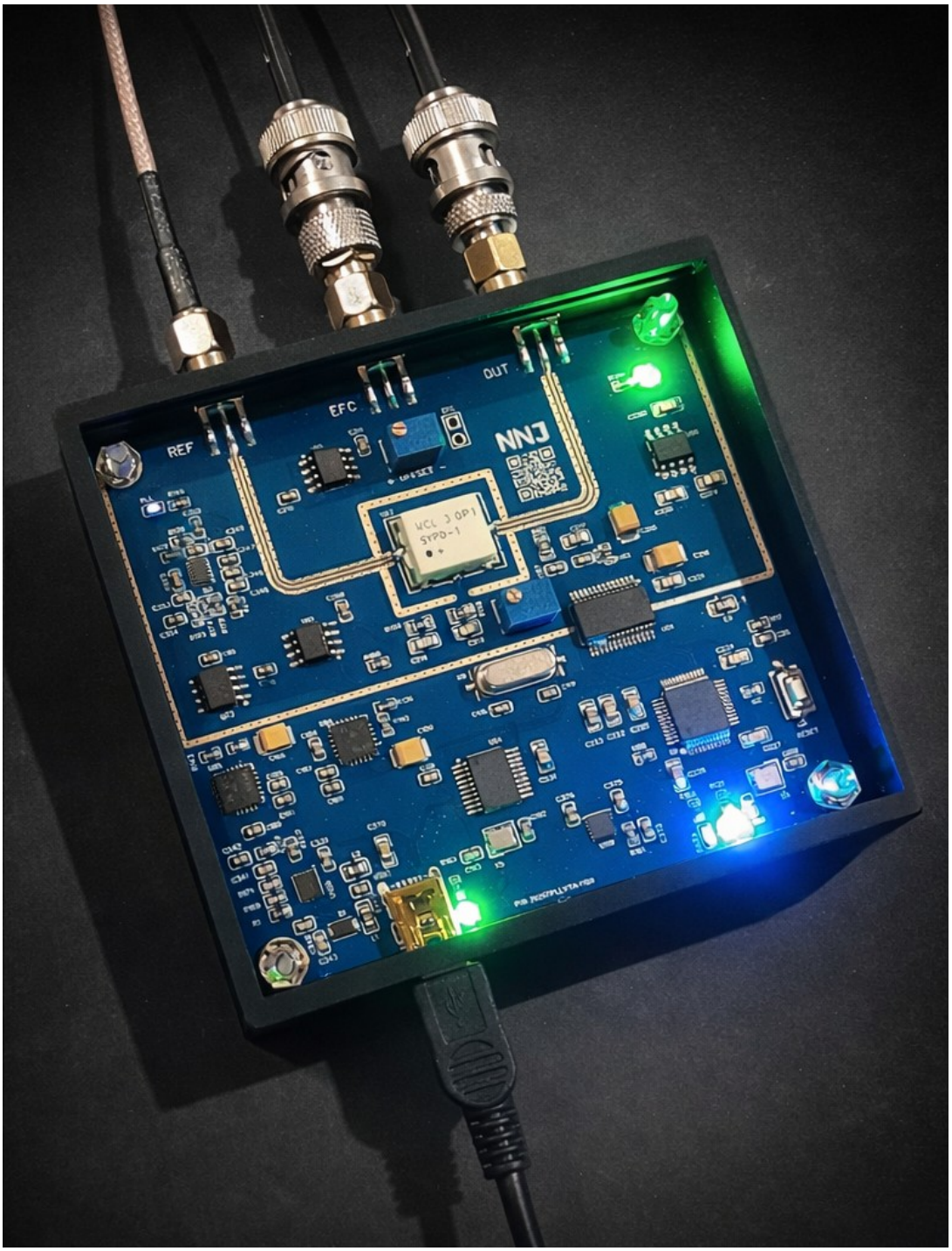
A compact, USB powered, Tight PLL for Frequency Metrology



This is a “product-for-fun” initiative—a personal design that evolved over the course of two years into a mature, production-ready instrument. Born from a deep fascination with high-stability frequency sources and the challenges of characterizing them accurately, the project was never intended for mass production. Instead, I decided to manufacture small quantities exclusively for passionate enthusiasts, researchers, and professionals who share an appreciation for precision metrology.

The instrument is specifically optimized for implementing the classic Tight Phase-Lock Loop (TPLL) technique, enabling detailed measurement of stability parameters in high-performance oscillators such as oven-controlled crystal oscillators (OCXOs), and even rubidium or higher standards. Thanks to the 24 bit ADC, it provides exceptional resolution for metrics including Allan deviation, phase noise, aging rates, warm-up characteristics, and short-term frequency fluctuations. The integration with John Miles’s Timelab is straightforward and can be used directly from the TPLLV1/A output .

At its core, the system is built on a compact four-layer printed circuit board that integrates a high-performance double-balanced mixer as phase detector (Mini-Circuits SYPD1+), precision analog signal conditioning with a dual op-amp (plus an additional buffer for the EFC output) , a 24-bit analog-to-digital converter (ADS1256), and an STM32F103 microcontroller for digital processing and output. The board features two SMA 50 Ω RF inputs for reference (REF) and device-under-test (DUT) signals, a buffered electronic frequency control (EFC) SMA output for loop closure, a UART serial interface that streams real-time frequency error directly in Hertz using a deliberate 1 Hz/V scaling convention.

A key aspect of the RF front-end layout is the consistent use of Grounded Coplanar Waveguide (GCPW) structures for both the REF and DUT input paths to the SYPD-1+ mixer. GCPW was specifically chosen to maintain precise 50 Ω characteristic impedance with low return loss and excellent signal integrity across the entire operating range. While the relatively modest frequencies involved (1 MHz to 100 MHz) do not strictly require such sophisticated transmission-line techniques—conventional microstrip routing would have been adequate—the adoption of GCPW provides significant advantages in a compact four-layer design: enhanced shielding through surrounding ground vias, reduced crosstalk between adjacent traces, lower susceptibility to substrate tolerances, and improved immunity to external interference. These benefits ensure that the phase detector receives clean, undistorted signals, contributing directly to the system’s low noise floor and high measurement fidelity. It is able to accepts both sinewaves and square waves (also mixed to each other — beware that phase noise will be obviously higher if you compare sines to squares)

The design philosophy prioritizes simplicity, repeatability, and precision. By carefully conditioning the phase detector voltage and applying a unity scaling factor, the system delivers frequency deviation readings that are numerically identical to the error voltage in volts—eliminating the need for complex, temperature-sensitive gain constants or frequent recalibration during typical operation. The instrument is fully calibrated and optimized for 10 MHz signals (the de facto standard for precision frequency references), while remaining usable across a broader range from approximately 1 MHz to 100 MHz with minor user-applied corrections for mixer offset at non-standard frequencies.

This article provides an in-depth technical description of the system, including its theoretical foundations, detailed hardware architecture, analogue and digital signal paths, firmware functionality, measured performance, practical applications, and availability.

**Background: The Tight Phase-Lock Loop Technique**

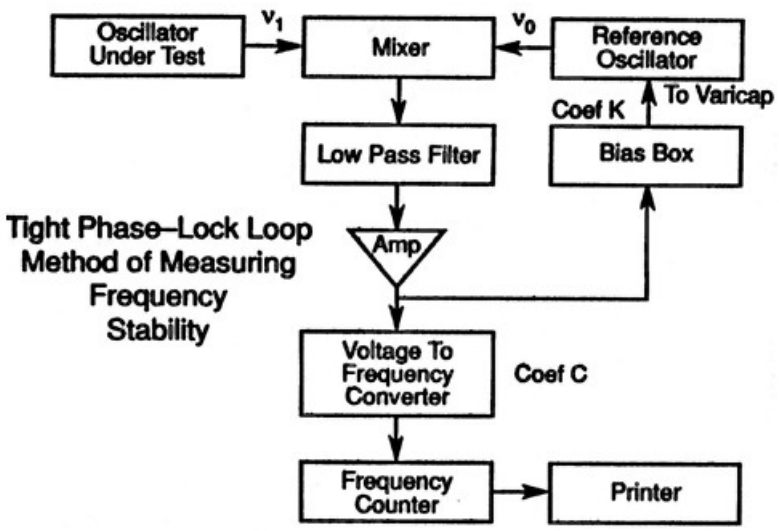



Figure 1.7

The evaluation of ultra-high-stability frequency sources has long relied on phase comparison techniques rather than simple frequency counting, primarily because counting methods are fundamentally limited by measurement gate time and counter resolution. Phase comparison methods, by contrast, offer far greater sensitivity by directly capturing the time-domain behavior between two oscillators.

Among these, the Tight Phase-Lock Loop (TPLL) method stands out for its elegance and achievable resolution. In this approach, two oscillators are phase-locked together with intentionally high loop gain and bandwidth. One oscillator serves as a stable reference, while the other is the device under test (DUT). The control voltage required to maintain phase coherence becomes a highly amplified representation of the DUT's instantaneous frequency deviations relative to the reference.

When the loop bandwidth significantly exceeds the Fourier frequencies of interest (i.e., the loop response time is much shorter than the averaging intervals being studied), the error signal transitions from representing phase fluctuations to directly representing frequency fluctuations. This integration effect is key: short-term noise and instabilities in the DUT are fully transferred to the control voltage, while the reference's contribution is suppressed by the loop's feedback action. Long-term drift can be isolated by appropriate biasing and filtering.

The technique has been a cornerstone of frequency metrology for decades. The NIST Time and Frequency Division provides a clear and authoritative description in their handbook on characterizing signal sources:

D. Tight phase lock loop method The second type of phase lock loop method is essentially the same as a loose phase lock loop except that in this case the loop is in a tight phase lock condition; i.e., the response time of the loop is much shorter than the sample times of interest—typically a few milliseconds. In such a case, the phase fluctuations are being integrated so that the voltage output is proportional to the frequency fluctuations between the two oscillators and is no longer proportional to the phase fluctuations (for sample times longer than the response time of the loop). A bias box is used to adjust the voltage on the varicap to a tuning point that is fairly linear and of a reasonable value. The voltage fluctuations prior to the bias box (biased slightly away from zero) may be fed to

a voltage to frequency converter which in turn is fed to a frequency counter where one may read out the frequency fluctuations with great amplification of the instabilities between this pair of oscillators. The frequency counter data are logged with a data logging device. The coefficient of the varicap and the coefficient of the voltage to frequency converter are used to determine the fractional frequency fluctuations, y_i, between the oscillators, where i denotes the ith measurement. It is not difficult to achieve a sensitivity of a part in $10^{14}$ per Hz resolution of the frequency counter, so one has excellent precision capabilities with this system.

Early implementations of the NIST method were predominantly analogue, relying on chart recorders, voltage-to-frequency converters, and mechanical bias adjustments. Later refinements by John Miles (KE5FX) with his accompanying software tools like TimeLab , modernized the approach by introducing digital data acquisition and automated post-processing.

The instrument described here represents a further evolution of this lineage. By replacing the traditional voltage-to-frequency converter and counter chain with direct 24-bit ADC digitization and microcontroller-based scaling, it eliminates multiple sources of conversion error and drift. The deliberate 1 Hz/V scaling aligns naturally with typical OCXO EFC sensitivities, allowing the serial data stream to provide instantaneous frequency deviation in Hertz without requiring per-setup calibration of varicap coefficients or intermediate converters. This direct readout greatly simplifies both real-time monitoring and long-term logging for subsequent Allan deviation analysis.

## System Overview

The TPLLV1/A is housed on a compact four-layer PCB measuring approximately 7 × 8 cm , designed for bench-top or integrated use. Key external interfaces include:

Two SMA connectors for 50 Ω RF inputs: REF (reference oscillator) and DUT (device under test)
One SMA connector for the buffered EFC output, providing a low-impedance, filtered error voltage suitable for direct connection to an oscillator’s control pin.
UART output (115200 baud, 8N1) streaming formatted data.
Multiple LEDs indicating : measurement activity (heartbeat) for PLL basic lock status , Tight Phase locked loop status (toggles -5000.0 to +5000.0 microvolts range), data output and Digital/Analogue power rails status.
USB Type Mini-B , with typical consumption less than 100 mA
The overall signal chain is straightforward yet highly optimized:

REF and DUT signals are applied to the LO and RF ports of a Mini-Circuits SYPD-1+ double-balanced mixer, producing a DC-rich IF output proportional to phase difference.
The IF signal undergoes multi-stage passive RC low-pass filtering to reject RF leakage and higher-order products.
A precision dual op-amp package processes the filtered signal: the first stage applies controlled gain to the error voltage, while the second stage provides low-impedance buffering to both the EFC output connector and one differential input pair of the ADS1256 ADC.
A parallel monitoring path routes the pre-amplification mixer output to the second differential input pair of the ADS1256, enabling simultaneous digitization of both raw and amplified error signals.
The STM32F103 microcontroller acquires data from the ADC, performs averaging and offset correction, applies the 1 Hz/V scaling to the primary amplified channel, and continuously streams frequency error (Hz) alongside diagnostic EFC voltage (µV).
This dual-channel measurement approach provides valuable flexibility: the amplified channel delivers the primary high-sensitivity frequency error readout, while the raw channel offers insight into mixer behavior and facilitates diagnostic troubleshooting.

## Operational Modes

The system supports two distinct modes of operation, offering flexibility for different metrology and disciplining tasks. In Mode A—the classic symmetric configuration for stability characterization—two oscillators of comparable performance (e.g., two same OCXOs or frequency references) are compared directly. Here, the REF input receives one oscillator, the DUT input the other, and the EFC output is connected to the control pin of the REF. This setup enables the traditional (Tight) Phase-Lock Loop measurement, where the logged frequency error reveals the relative instabilities between the pair, ideal for computing Allan deviation or isolating individual oscillator contributions ,

In Mode B—the asymmetric disciplining configuration—the system is used to lock a lower-stability source (e.g., an OCXO or TCXO) to a higher-accuracy reference (e.g., a rubidium standard, caesium beam, or GPS-disciplined oscillator). Importantly, the input assignments are reversed compared to Mode A: the high-accuracy source is connected to the DUT input, while the less stable oscillator (the one to be disciplined) is connected to the REF input, with its EFC pin driven by the board's output. This reversal ensures correct loop polarity—the error voltage drives the REF oscillator toward coherence with the superior DUT reference. In this mode, the system effectively transfers the short- and medium-term stability of the high-accuracy source to the disciplined oscillator, while leveraging the long-term accuracy of GPS or atomic standards. The streamed frequency error data remains valid in both modes.

## Hardware Design

RF Front-End and Analog Signal Conditioning
The RF section is dominated by the Mini-Circuits SYPD-1+ double-balanced mixer, chosen for its wide bandwidth (specified 1 to 100 MHz), high isolation, and low conversion loss.

Immediately following the mixer's IF port, a double cascaded RC low-pass filter provides aggressive attenuation of residual RF leakage, sum-frequency components, and high-frequency noise. The corner frequencies are carefully chosen to support loop bandwidths while preserving low group delay and excellent DC stability.

The core of the analog section is built around the Analog Devices ADA4898 family of op-amps, selected for their excellent performance in precision and high-dynamic-range applications: ultra-low voltage noise (typically 0.9 nV/√Hz), very low distortion, high slew rate (55 V/µs), microvolt-level offset, and picoamp bias currents. These characteristics ensure negligible contribution to the system noise floor and faithful, linear amplification of the delicate phase detector signal.

The signal flow is as follows:

After the initial double RC filtering, the mixer output is fed to the first channel of an ADA4898-2 dual op-amp configured as a non-inverting amplifier. Gain is user-adjustable via a precision potentiometer, allowing the typical phase excursions to be mapped to a convenient full-scale voltage range while maintaining linearity and avoiding saturation under normal operating conditions.
The amplified output is then routed in parallel:
To the second channel of the same ADA4898-2, configured as a unity-gain buffer. This buffered signal passes through additional passive RC filtering (for enhanced loop stability and noise reduction) before driving one fully differential input pair of the ADS1256 ADC.
To a separate ADA4898-1 single op-amp, also configured as a pure unity-gain buffer, which provides a low-impedance drive to the external EFC output connector.

This architecture delivers both a high-gain, conditioned error signal for high-resolution digital capture and a clean, low-impedance analog EFC voltage for direct loop closure, while leveraging the outstanding noise and precision performance of the ADA4898 family throughout the signal chain. A parallel unamplified path directly from the mixer output also feeds the second differential ADC pair for diagnostic monitoring .

The Texas Instruments ADS1256 24-bit delta-sigma ADC is configured for fully differential operation on both channel pairs, using a precision 2.5 V external reference. Operating at its 1000 SPS data rate with internal averaging, the ADC delivers exceptional noise performance.

**Power Supply and Grounding Design**

A significant challenge in achieving the targeted microvolt-level noise floor lies in power supply integrity, particularly given the mixed-signal nature of the design and the requirement for USB powering. The board employs four separate low-dropout regulators (LDOs) to generate isolated rails for different functional blocks, ensuring minimal crosstalk and exceptionally clean supplies despite the modest total consumption.

Primary 5 V input from USB is first filtered and then distributed to:

A dedicated digital LDO for the STM32F103 and associated logic.
Separate LDOs for the ADS1256 digital interface and reference circuitry.
A positive analog LDO feeding analog functions.
The most critical—and layout-intensive—portion is the analog frontend supply, which requires true bipolar rails for the dual op-amp and associated filtering. This is accomplished using the Texas Instruments LM27762, a charge-pump-based dual-output regulator that generates stable +5 V and –5 V rails from a single positive input with very low noise.

Routing , powering and laying out the LM27762 proved to be one of the most challenging aspects of the PCB design process. Multiple iterations (and also separate PCB design blocks) were required to optimize correct flying capacitor placement , dedicated power/ground islands, and extensive local bypassing.

Compounding the difficulty, the analog and digital grounds are intentionally separated across the four-layer stackup—analog ground occupying a dedicated split plane connected to digital ground at a single star point near the power entry. This classic mixed-signal partitioning prevents digital switching currents from contaminating the analog reference, but requires extreme care in component placement and routing to avoid creating unintended ground loops or slot antennas that could pick up RF leakage from the mixer section.

**Digital Section and Firmware Implementation**

The digital core is an STM32F103C8T6 microcontroller, selected for its balance of performance , peripheral richness and widespread development tool support.

The firmware is implemented in C using the STM32 standard peripheral library and is deliberately kept minimal and deterministic—no operating system or interrupt-heavy architecture—to ensure low jitter and predictable timing in the measurement loop.

Upon power-up, the firmware initializes the system clock, GPIO configurations, UART peripheral (115200 baud, 0.1s output rate), and the ADS1256 via SPI. It then enters an infinite main loop that

continuously acquires data from both differential ADC channels at the full 1000 samples-per-second rate.

For each measurement cycle, eight consecutive samples from each channel are accumulated and averaged, providing substantial noise reduction and yielding an effective update rate of approximately 10 Hz. The raw ADC codes are converted to voltages using the precise bipolar differential formula incorporating the 2.5 V reference.

A small fixed DC offset correction is subtracted from the primary amplified channel to null residual mixer imbalance at the design frequency of 10 MHz , according to the SYPD-1+ datasheet specs. The amplified channel voltage is directly interpreted as frequency error in Hertz via the 1 Hz/V convention..

Formatted data lines are streamed continuously over UART, with simple GPIO-driven LEDs providing visual feedback with the following typical output , where column 1 is the frequency and column 2 is the voltage reading from the mixer output:

1.790728e+00 -3359.046173
1.783133e+00 -3453.221512
1.791057e+00 -3301.825714
1.791064e+00 -3484.215927
1.777067e+00 -3485.408020
1.776427e+00 -3561.105919
1.776253e+00 -3513.422203
1.770705e+00 -3637.399864
1.763964e+00 -3694.620323

This streamlined approach ensures robust, repeatable performance while remaining easily modifiable.

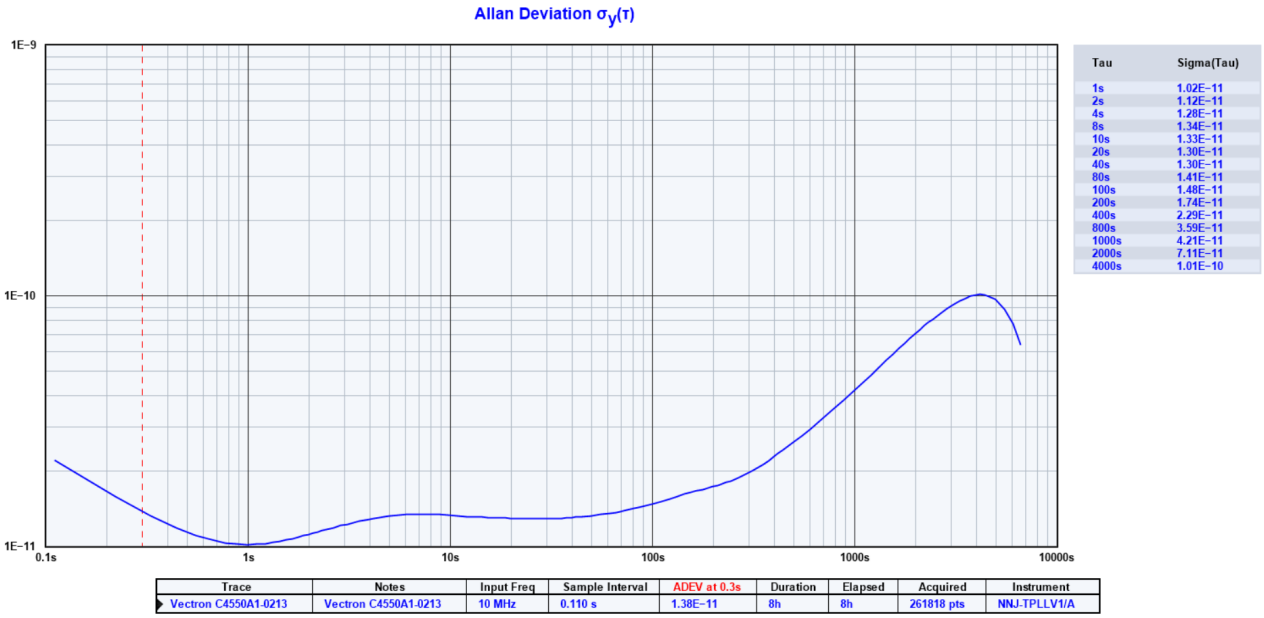
**Tests and performances**

Extensive bench testing at 10 MHz demonstrates sub-Hertz resolution , with system noise floor supporting fractional frequency measurements consistent when compared to “classic” time interval counters or similar professional systems.

Below are some tests carried out using a couple Vectron C4550A1-0213, over a total duration of eight hours.
Even though this system delivers maximum efficiency in short- to medium-term stability analysis, and this capture already spans several hours, it is still possible to observe important details that are not always accessible with a conventional time interval counter.

For example, it allows the true nature of the oscillator’s short-term stability ($\tau$ = 1 s to 10 s) to be observed, as well as the actual long-term drift. A substantial number of devices of significant technical interest exhibit short-term stability that cannot be directly measured using a time-interval counter indeed.

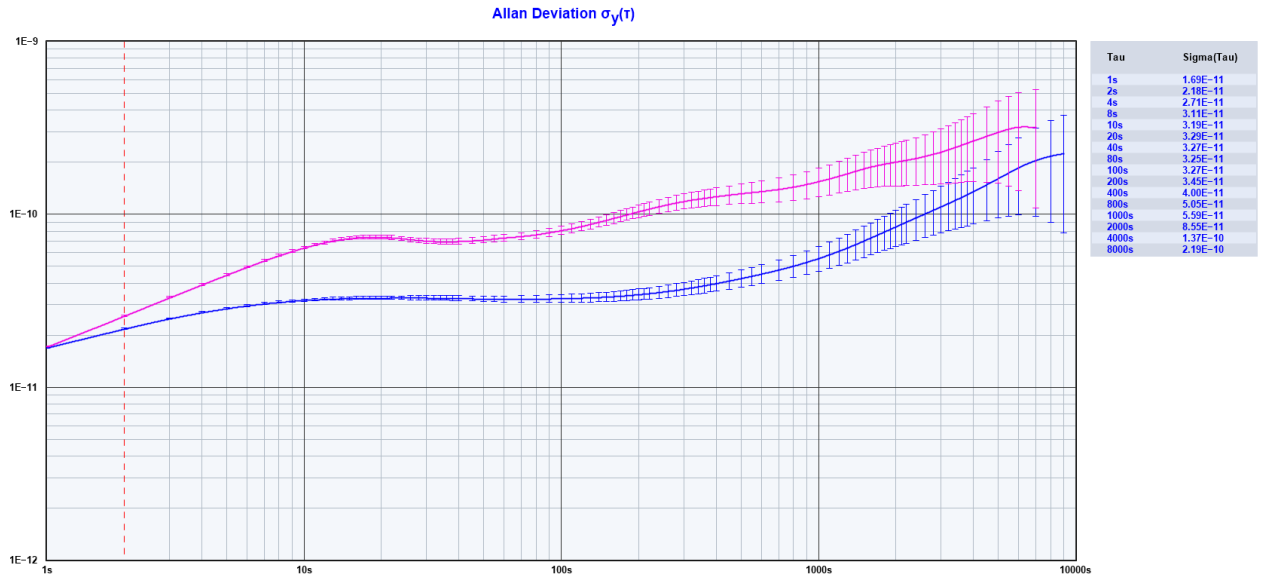
Note: This measurement was performed using two identical OCXOs, mounted on a dedicated board, powered by a regulated supply, enclosed in a proper metal housing, and left powered on for more than 48 hours before starting the measurement.




| Tau | Sigma(Tau) |
|---|---|
| 1s | 1.02E−11 |
| 2s | 1.12E−11 |
| 4s | 1.28E−11 |
| 8s | 1.34E−11 |
| 10s | 1.33E−11 |
| 20s | 1.30E−11 |
| 40s | 1.30E−11 |
| 80s | 1.41E−11 |
| 100s | 1.48E−11 |
| 200s | 1.74E−11 |
| 400s | 2.29E−11 |
| 800s | 3.59E−11 |
| 1000s | 4.21E−11 |
| 2000s | 7.11E−11 |
| 4000s | 1.01E−10 |

| Trace | Notes | Input Freq | Sample Interval | ADEV at 0.3s | Duration | Elapsed | Acquired | Instrument |
|---|---|---|---|---|---|---|---|---|
| Vectron C4550A1-0213 | Vectron C4550A1-0213 | 10 MHz | 0.110 s | 1.38E−11 | 8h | 8h | 261818 pts | NNJ-TPLLV1/A |

This is the direct comparison using an Agilent 53220A versus a GPSDO ( https://ampnuts.ru )

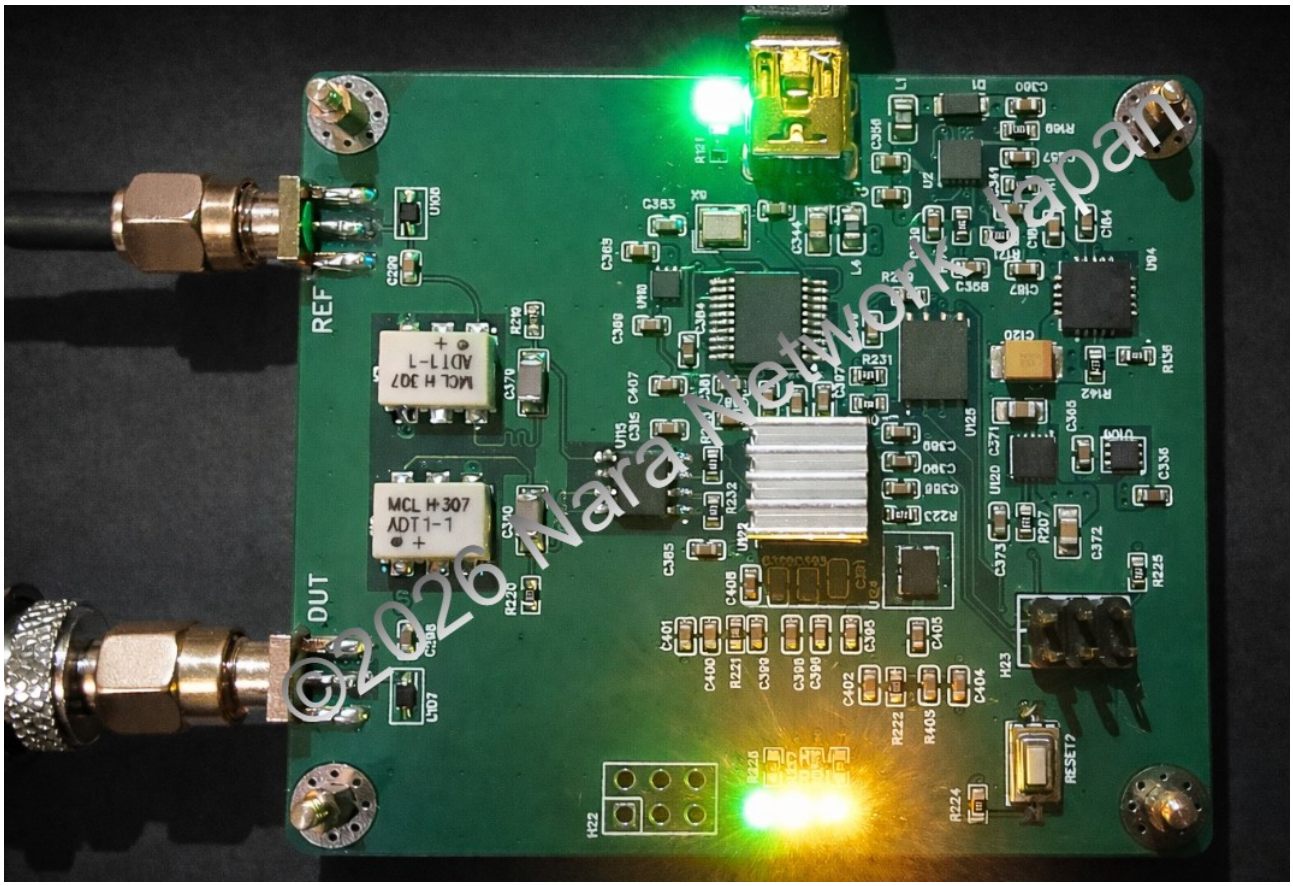



| Tau | Sigma(Tau) |
|---|---|
| 1s | 1.69E−11 |
| 2s | 2.18E−11 |
| 4s | 2.71E−11 |
| 8s | 3.11E−11 |
| 10s | 3.19E−11 |
| 20s | 3.29E−11 |
| 40s | 3.27E−11 |
| 80s | 3.25E−11 |
| 100s | 3.27E−11 |
| 200s | 3.45E−11 |
| 400s | 4.00E−11 |
| 800s | 5.05E−11 |
| 1000s | 5.59E−11 |
| 2000s | 8.55E−11 |
| 4000s | 1.37E−10 |
| 8000s | 2.19E−10 |

| Trace | Notes | Input Freq | ADEV at 2s | Elapsed | Acquired | Instrument |
|---|---|---|---|---|---|---|
| Third run(covered) (Unsaved) | "VECTRON C4550A1-0213" VS "HP Z3805A GPSDO" | 10 MHz | 2.18E−11 | 10h 58m 18s | 39052 pts | Agilent 53220A |
| Second run (after 10h) | "VECTRON C4550A1-0213" VS "HP Z3805A GPSDO" | 10 MHz | 2.59E−11 | 8h 22m 18s | 30138 pts | Agilent 53220A |

The exact test conditions employed in ampnuts' report are not known; nevertheless, despite the observed correlation, an independent verification was performed using a custom FPGA-based measurement system developed by myself (more to follow on this in the future). The system implements a time-interval counter based on a 100 MHz coarse counter, combined with carry-chain-based tapped delay lines to provide fine time resolution using an iCE40HX8K FPGA.

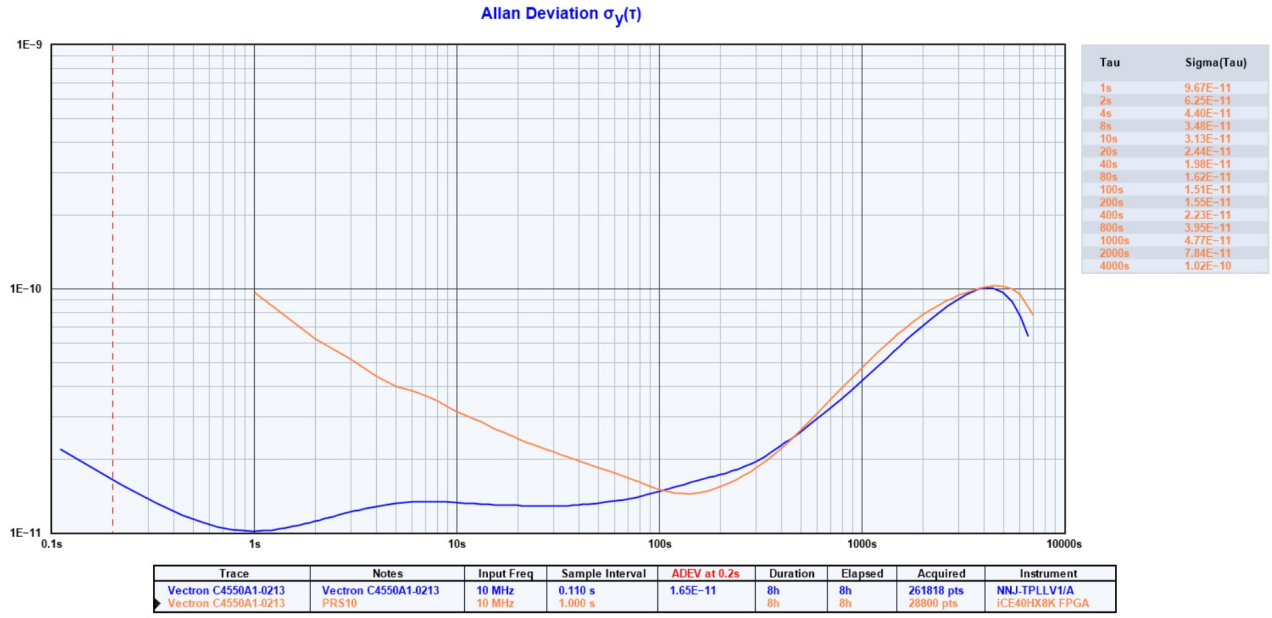
Here is a picture of the ongoing dev-prototype (REV A) that might be available in the future.





Measurements were conducted on the same OCXO previously tested with the TPLLV1/A, while employing an independent reference source, specifically a PRS10 rubidium frequency standard. The REF and DUT signal edges are timestamped independently, and their relative time difference is periodically computed and reported for phase and frequency-stability analysis.

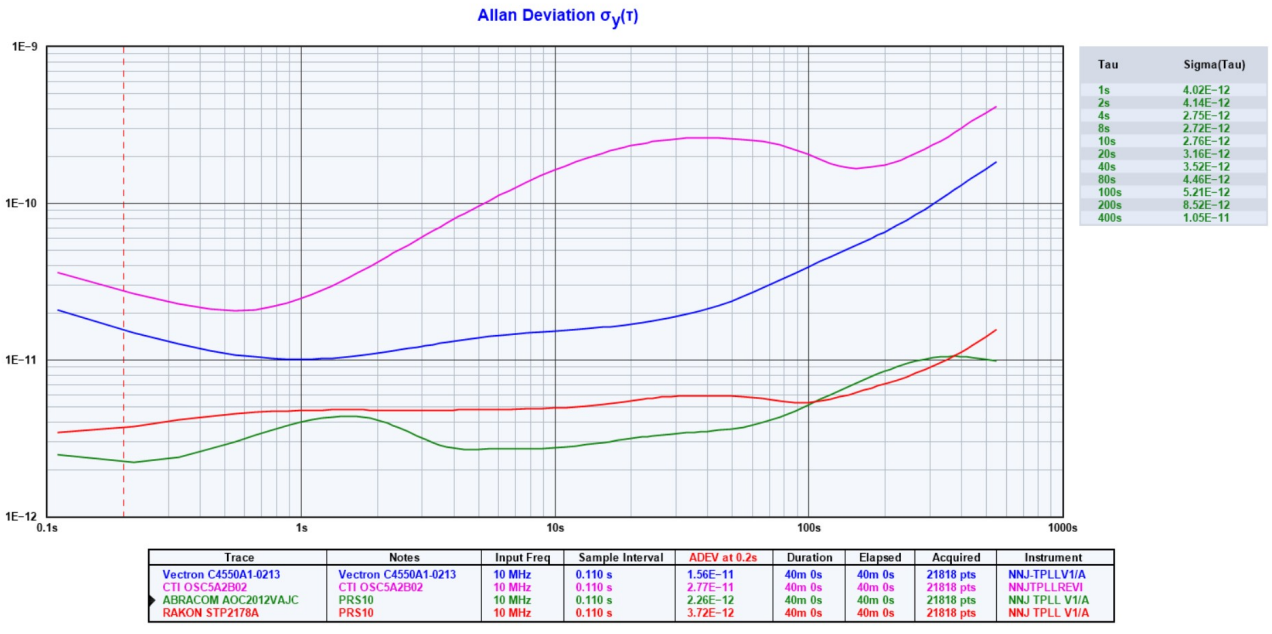
The excellent agreement observed for $\tau > 10$ s, despite the use of a different reference standard and an entirely independent hardware platform, provides strong confirmation of the validity of the measurement system.




The measurements reported below were performed using a variety of available oscillators. Some devices were evaluated in a “pure” TPLL configuration, in which identical OCXOs were used for both the DUT and reference paths, while others were measured using a PRS10 rubidium frequency standard as the reference.

In the latter case, a small, precisely controlled frequency (voltage) compensation was applied to the DUTs in order to align them with the rubidium reference. This procedure is standard practice when comparing a lower-stability source against a significantly more stable reference, such as a rubidium or higher-grade standard, to ensure proper phase locking and meaningful phase-difference measurements.

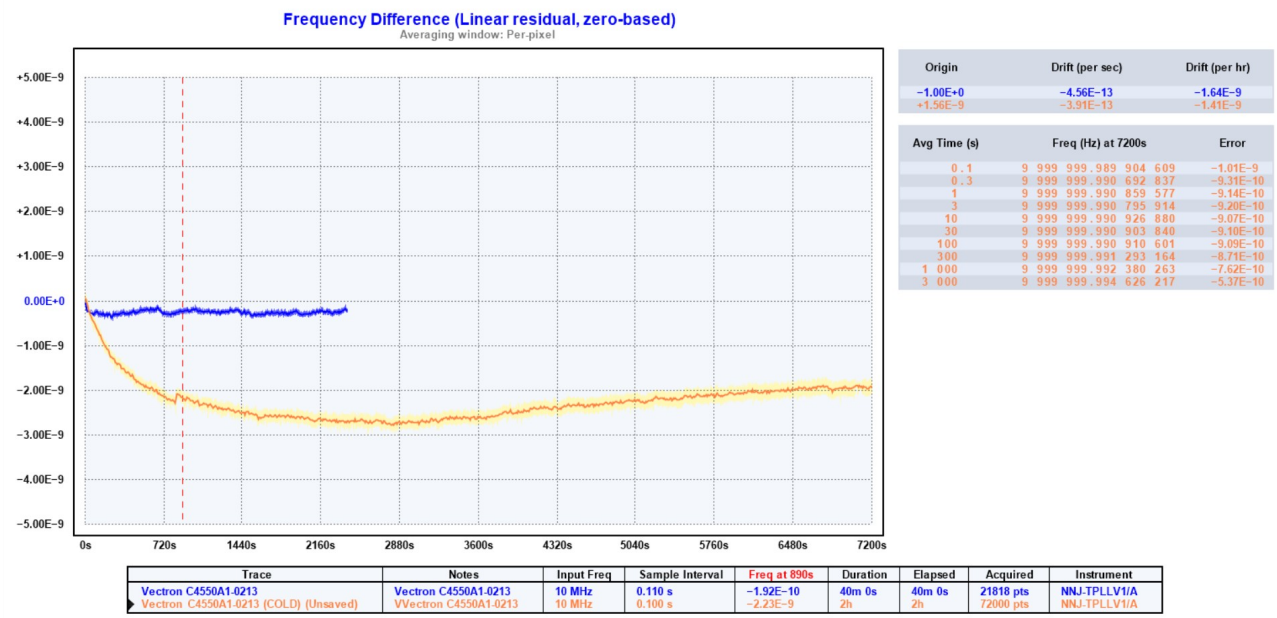
The Abracon oscillator was a new, unused device, mounted on a dedicated test board for these measurements.

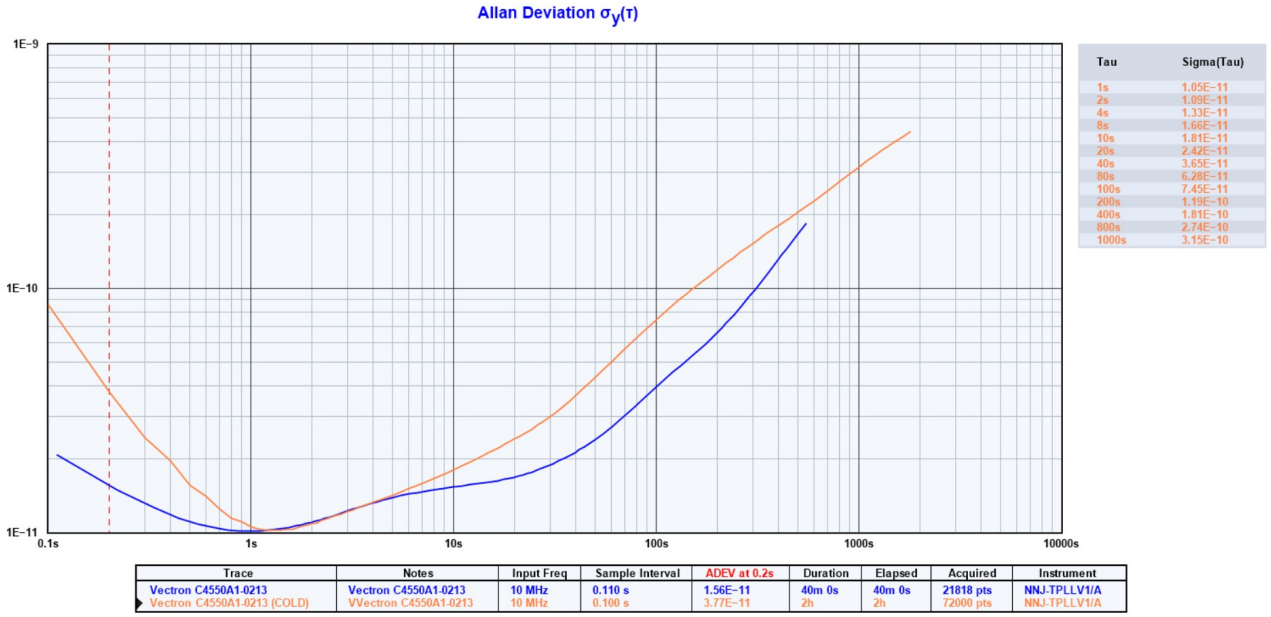


## Oscillator Drift and Warm-Up Characterization

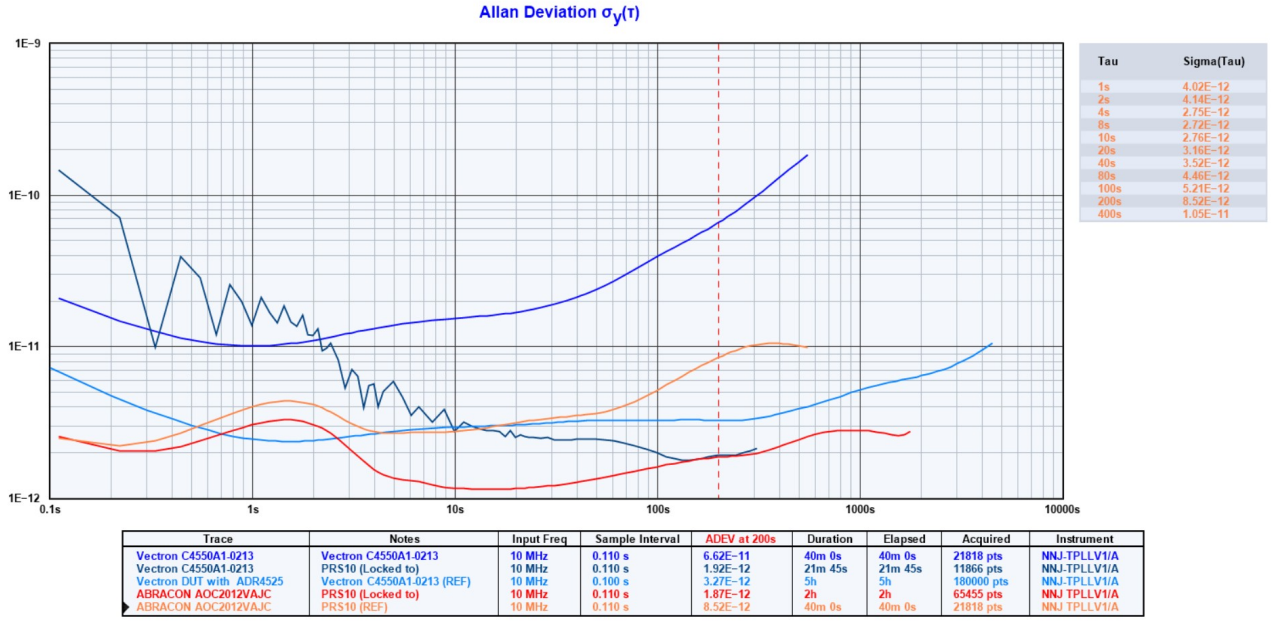
One of the most practical and revealing applications of the TPLLV1/A is its ability to effortlessly capture short-to-medium-term frequency drift (but also long one as well with proper conditions) and warm-up behavior in oscillators—phenomena that are critical for understanding real-world performance but often tedious to measure with conventional tools. By simply logging the streamed frequency error data over extended periods (hours to days), users can generate precise drift curves without additional instrumentation or complex setups.

A compelling example is shown in the accompanying plot of frequency difference (linear residual, zero-based) for the same OCXO measured under two conditions. The orange trace represents the oscillator immediately after a cold start: it exhibits a clear initial retrace drift of approximately 3–4 $\times 10^{-9}$ over the first ~2000 seconds, gradually settling toward a stable plateau as the oven and crystal reach thermal equilibrium. In contrast, the blue trace—captured from the same unit after 48 hours of continuous operation—remains remarkably flat near zero (within $\pm 5 \times 10^{-10}$), illustrating the dramatically improved stability once fully warmed up. This side-by-side comparison highlights not only the magnitude of warm-up effects but also the system's sub-$10^{-10}$ resolution in tracking slow drifts, making it straightforward to quantify retrace errors, aging rates, or environmental sensitivities. The ease of such measurements—requiring only the serial output from the device itself—democratizes high-precision metrology, allowing enthusiasts and researchers alike to uncover subtle behaviours that would otherwise demand far more sophisticated (and expensive) test equipment.






## Operating Modes and Reference Conditioning Effects




This image illustrates a comparative Allan deviation analysis obtained using the TPLLV1/A under three distinct operating conditions, highlighting both the flexibility and the intrinsic performance limits of the system.

The blue trace (Trace N.1 from top to bottom in the list) corresponds to the baseline measurement previously discussed in this work. In this configuration, the TPLLV1/A operates in its standard mode, comparing two identical Vectron C4550A1-0213 OCXOs in a symmetric “pure” TPLL arrangement. This trace therefore represents the intrinsic short- and mid-term stability achievable when both the reference and DUT exhibit closely matched performance.

Trace N.2 was obtained with the TPLLV1/A operating in Mode B, in which the Vectron OCXO is phase-locked to an external PRS10 rubidium frequency standard. In this case, the observed Allan deviation exhibits a more pronounced point-to-point variability, resulting in a visibly more irregular profile. This behaviour does not indicate degraded performance of the TPLLV1/A; rather, it reflects the interaction between the OCXO's control loop dynamics and the significantly higher long-term stability of the rubidium reference. When a lower-stability oscillator is tightly disciplined to a much more stable source, the residual phase-error sequence is dominated by control action, quantization effects, and loop bandwidth limitations, which manifest as increased local variance in the ADEV at shorter τ.

Trace N.3 represents a variant of the baseline configuration in which the DUT frequency control input (EFC) is biased using an external precision voltage reference, specifically the ADR4525. In this configuration, the reference voltage applied to the EFC was carefully set to align the OCXO's free-running frequency while minimizing control noise injection. The ADR4525 is a high-precision, low-noise voltage reference, specified with ±0.02 % initial accuracy, low temperature coefficient (as low as 2 ppm/°C), low output noise (≈1 µV p-p from 0.1 Hz to 10 Hz), and excellent long-term drift characteristics . These properties make it particularly well suited for biasing sensitive OCXO control inputs, where voltage noise and drift directly translate into frequency instability.

As shown, the use of the ADR4525 results in a noticeably smoother and lower Allan deviation at short tau compared to the rubidium-locked case, confirming that careful conditioning of the OCXO control voltage can significantly improve effective stability when operating near the oscillator's intrinsic noise floor.

It should be emphasized, however, that the ultimate performance remains bounded by the intrinsic tuning sensitivity and physical limitations of the OCXO itself. While the TPLLV1/A provides a highly flexible and low-noise platform capable of operating with identical oscillators, external atomic references, or precision voltage-biased configurations, the achievable stability is fundamentally limited by the DUT's ability to faithfully follow the applied reference or control signal. The confirmation is the almost perfect coherence at τ >100s of the ABRACON AOC2012VAJC: Trace N.4 locked to the PRS10 (MODE B) matching with the Vectron locked to the Rubidium (trace N.2), while trace N.5 free running using as REF the Rubidium locked into the ABRACON.

## Sensitivity to Environmental Conditions

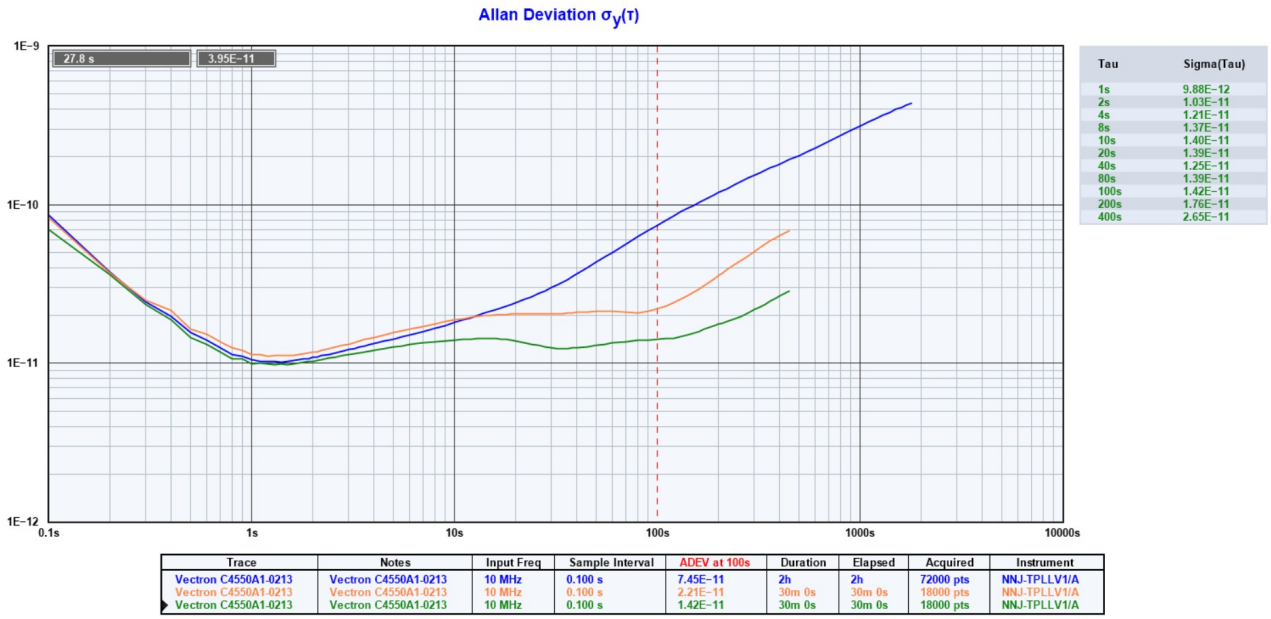



Figure above presents an additional Allan deviation comparison obtained using the same Vectron C4550A1-0213 OCXO, intended to illustrate the sensitivity of the TPLLV1/A measurement system to environmental and thermal conditions.

Trace 1 corresponds to a cold-start condition already showed previously, acquired shortly after power-up. As expected, the Allan deviation is dominated by transient thermal effects and warm-up drift, resulting in elevated instability at medium and long averaging times.

Trace 2 was obtained after the system reached thermal equilibrium with both OCXOs operating inside an open enclosure. Under these conditions, both short-term and long-term performance remains influenced by residual air currents and incomplete thermal shielding.

Trace 3 represents the same configuration with the OCXOs enclosed within a fully closed metal housing. This arrangement provides enhanced thermal isolation and mechanical shielding, yielding a clear reduction in Allan deviation over a wide range of τ and producing the most stable and repeatable result among the three cases.

The clear separation between these traces demonstrates the high sensitivity and resolution of the TPLLV1/A, enabled in part by its 24-bit ADC–based phase and control measurement architecture and low-noise signal chain. Subtle differences in thermal and environmental conditions, often obscured in conventional PLL or counter-based measurements, are readily resolved here.

These results confirm that the TPLLV1/A is not only suitable for absolute stability measurements, but also serves as a powerful diagnostic tool for evaluating warm-up behavior, enclosure effectiveness, and environmental coupling in high-performance OCXO-based systems.

**Availability**

Given its origins as a passion project, this instrument is produced in limited small-batch runs by Nara Network Japan and offered exclusively for now through our website at www.naranetwork.com. Each unit is individually assembled, tested, and calibrated in our modest Sapporo laboratory. Prospective buyers should anticipate fulfilment times of up to 25 days to allow for careful quality control and component sourcing.